Computer Logic 1 – Practical 1

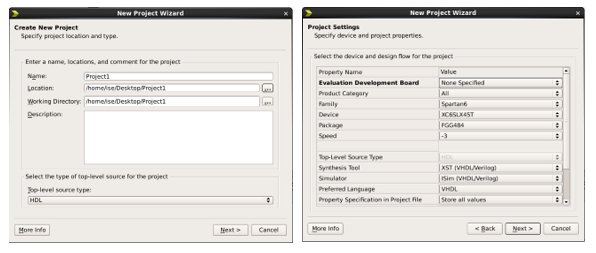
**Objective**:

To use the *Xilinx ISE Design Suite* to simulate simple combinational circuits.

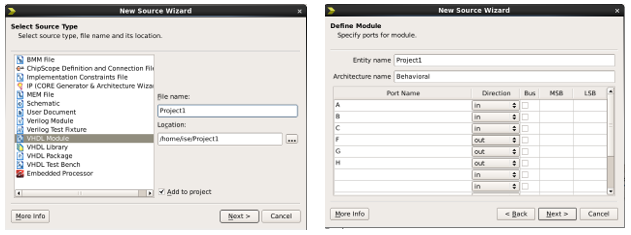
**Tasks**:

1. The *Xilinx ISE environment* was opened on the Linux virtual machine and a new project was created using the menu item *File ~> New Project*. The project was then called “*Project1*” and it was set to be stored in a particular location. Then, the following options were chosen (whilst others were left unchanged):

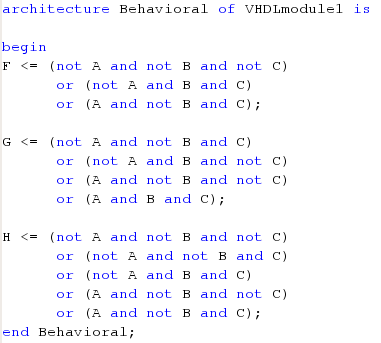
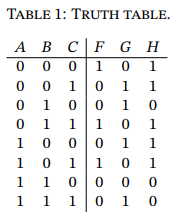
* Top-level source type: HDL
* Family: Spartan6
* Device: XC6SLX45T
* Package: FGG484
* Synthesis tool: XST (VHDL/Verilog)
* Simulator: Isim (VHDL/Verilog)
* Preferred language: VHDL



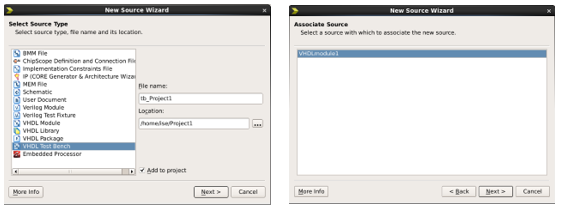
1. A new source file was then created using the menu item *Project ~> New Source*. The new source was of type VHDL Module and 3 input(A, B, C) and another 3 output(F, G, H) ports were assigned as shown.



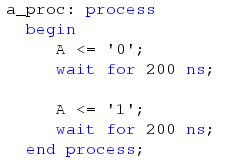
1. In the architecture body, VHDL code was added to set the inputs to correspond to Truth Table 1. The truth table and code inputted are shown below:



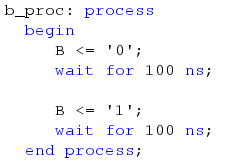
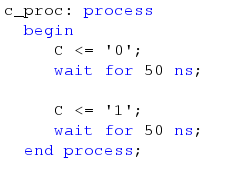
1. After the VHDL code was entered, functional simulation was performed. This was done by generating a test bench:
2. A new file called *tb\_Project1* was created from menu item *Project ~> New Source*. The source type was set to *VHDL Test Bench* and the original VHDL file *Project1* was associated with this newly created one.



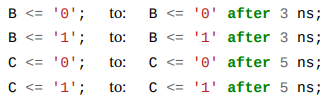
1. Parts of the test bench usually used for clock were eliminated as they were irrelevant to this particular design.
2. The stimulus process was replaced with the following code:



1. Other processes were then written to stimulate B and C as shown:

1. The *Simulation* view in the top left panel was then selected, followed by the *Behavioral* simulation. The test bench was then selected and the *Simulate Behavioral Model* option in the process panel was chosen.
2. The outputs were checked to correspond to *Truth Table 1*.
3. The test bench file was then modified with some artificial glitches and saved.



1. The design was simulated once more.
2. In this case, some glitches known as hazards were introduced. There were 2 types:
3. Static hazards: Those having the same levels before and after

(initial value ‘1’, followed by short ‘0’ and final value is ‘1’ again)



1. Dynamic hazards: Those having different levels before and after

(initial value ‘0’, followed by a short ‘1’ and another short ‘0’ and final value is ‘1’)



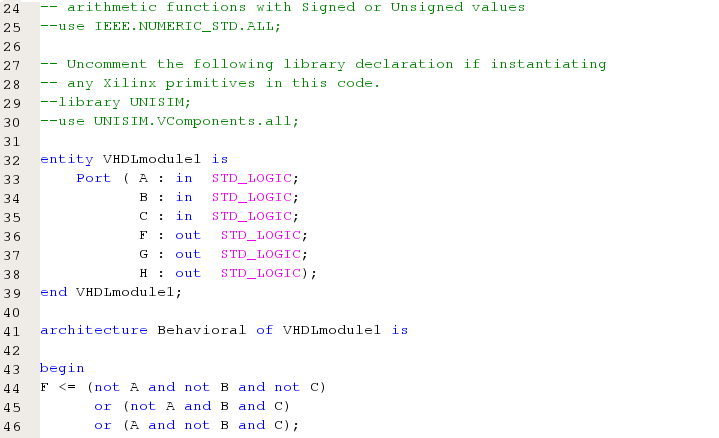
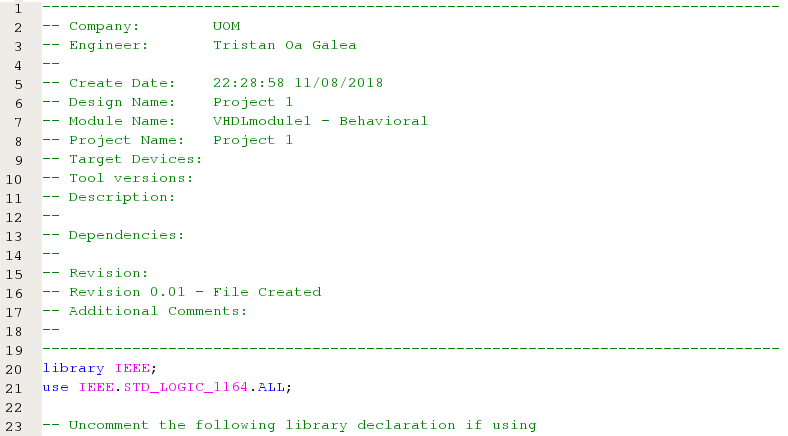
These hazards were caused by the artificial glitches introduced in step 7.

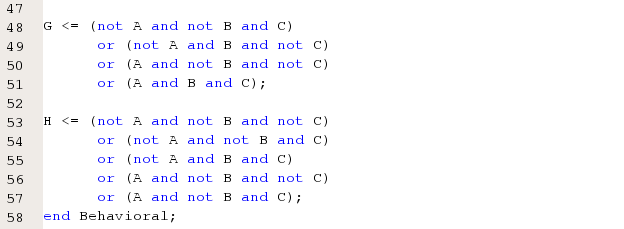
An example of a static hazard in this Project would be: Outputs *F* and *G* between 100 – 110 ns.

An example of a static hazard in this Project would be: Outputs *F* and *G* between 190 – 210 ns.

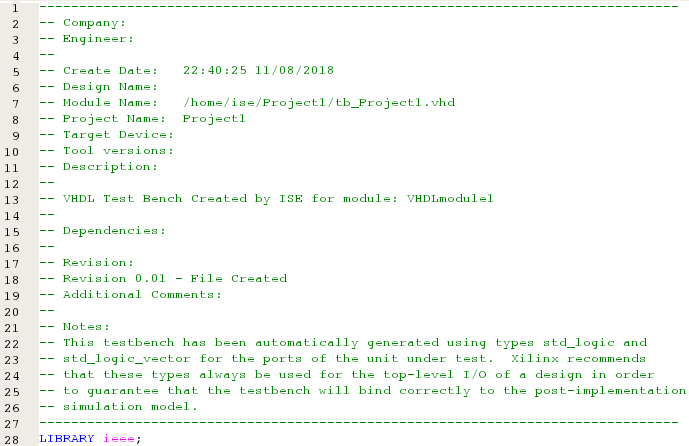
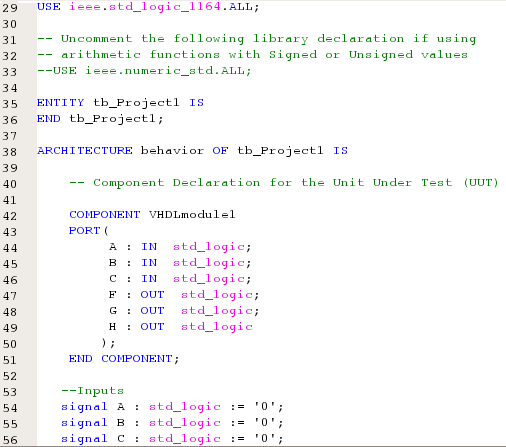
**Appendix (Code):**

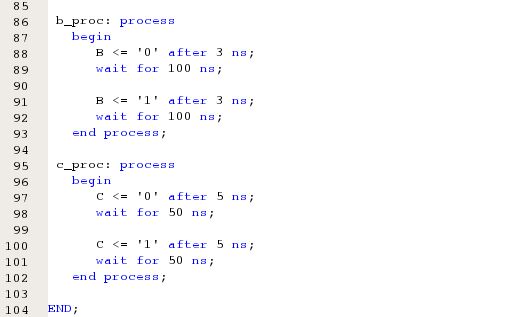
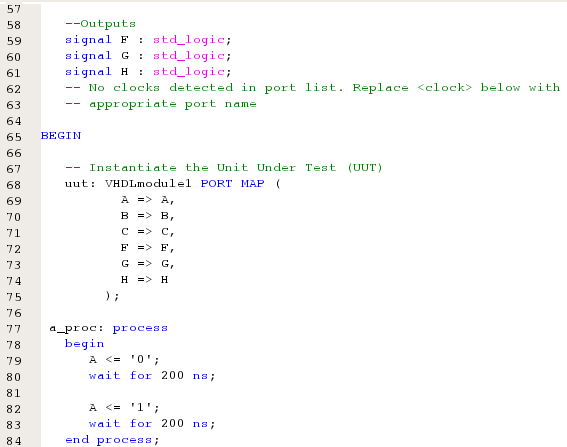
**VHDL Module (Project1):**





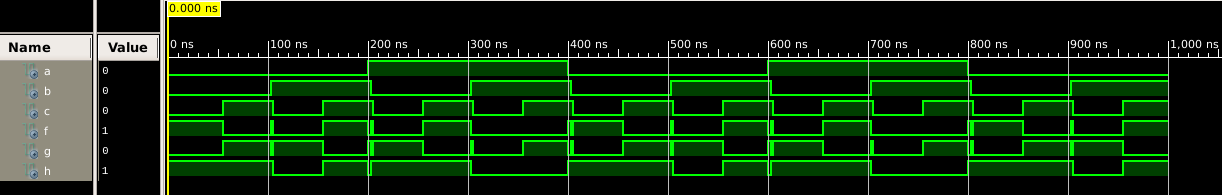
**VHDL Test Bench (tb\_Project1):**



**Simulated Behavioral Model:**

**(With glitches)**



**Conclusion:**

*Xilinx ISE Design Suite* was successfully used to simulate simple combinational circuits.